



Intel 82379AB (SIO.A) System I/O Component Specification Update

Release Date: May, 1996

The Intel 82379AB (SIO.A) System I/O component may contain design defects or errors known as errata. Characterized errata that may cause the Intel 82379AB (SIO.A) System I/O component's behavior to deviate from published specifications are documented in this specification.

Order Number 297734-001

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REVISION HISTORY

Date of Revision	Version	Description
May, 1996	-001	This document is the first revision of the Intel 82379AB (SIO.A) System I/O Component Specification Update.

PREFACE

This document is an update to the specifications contained in the *Intel 82378ZB System I/O (SIO) and 82379AB System I/O APIC (SIO.A) Datasheet (order number 290571)*. It is intended for hardware system manufactures and software developers of applications, operating systems or tools. It contains Specification Changes, Errata, Specification Clarifications, and Documentation Changes.

Nomenclature

Specification Changes are modifications to the specifications of the 82379AB System I/O APIC (SIO.A). These modifications will be reflected in the future releases of the affected specification.

Errata are design defects or errors. Characterized errata may cause 82379AB System I/O APIC (SIO.A)'s behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Clarifications describes a specification in greater detail or highlights complex design situations that may require implementation changes.

Documentation Changes include typos, errors, or omissions from the published specification of the 82379AB System I/O APIC (SIO.A). The changes will be incorporated in the next revision of the document.

S-Specs are temporary exceptions to the published standard specifications.

Component Marking Information

Stepping	S-Spec	Top Marking	Freq.	Notes
A-1		S, 82379AB	33	Production

Component Identification via Programming Interface

PCI Register	PCI Offset	Value
Vendor ID	00-01h	8086h
Device ID	02-03h	0007h
Revision Number	08h	88h

SUMMARY TABLE OF CHANGES

The following table indicates the Specification Changes, Errata, Specification Clarifications, and Documentation Changes which apply to all currently available stepping and planned steppings. Intel intends to fix some of the errata in a future stepping of the component, and to account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

CODES USED IN SUMMARY TABLE

X:	Specification Change or Clarification that applies to this stepping or to this product line.
Doc:	Document change or update that will be implemented.
Fix:	This erratum is intended to be fixed in a future step of the component.
Fixed:	This erratum has been previously fixed.
NoFix	There are no plans to fix this erratum.
(No mark) or (Blank Box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.
Shaded:	This erratum is either new or modified from the previous version of this document.

82379AB (SIO.A)

No.	A1	Plans	430NX	450	SPECIFICATION CLARIFICATION
1	X	No Fix	X	X	Lack of 3.3V Buffered Signals.

SPECIFICATION CHANGES

There are no Specification Changes to include in this revision.

ERRATA

There are no Errata to include in this revision.

SPECIFICATION CLARIFICATIONS

1. *Lack of 3.3V Buffered Signals*

NONE of the SIO.A signals use 3.3V output buffers. INT, NMI, IGNNE#, SMI#, ALT_A20, STPCLK#, and ALT_RST# will need external 3.3V drivers if used with CPUs that do not have 5V tolerant inputs.

APICD[1:0] are open-drain I/Os. They require external pull-ups (330 Ω recommended) to the 3.3V rail.

DOCUMENTATION CHANGES

There are no Documentation Changes to include in this revision.